

## SYSTEM PAGE REF.

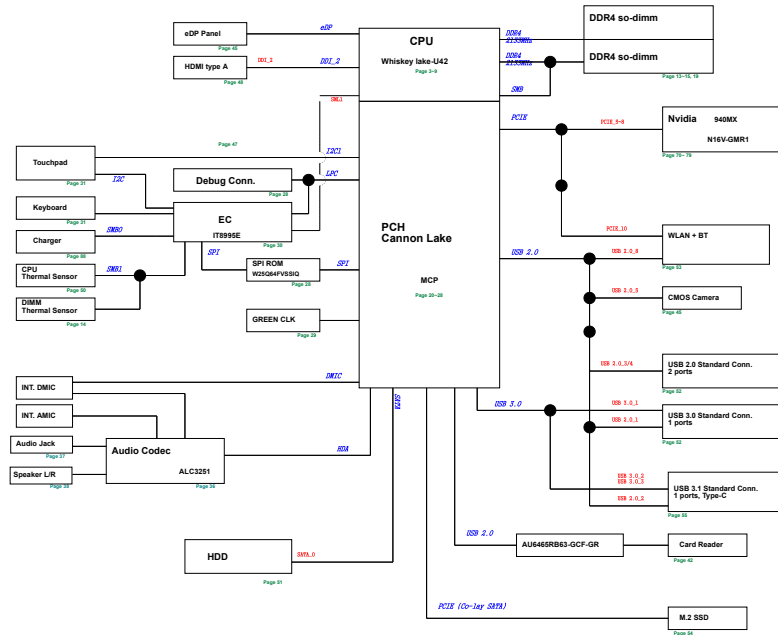
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83	PW_I/O_DDR (RT8202A+uP7711)
84	PW_LDO_+1.8V9 (LDO)
85	PW_CPU_VIDA_CORE (RT8202A)
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## BLOCK DIAGRAM

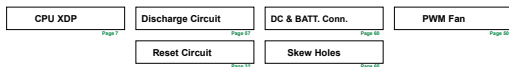
## X530FN\_2.2

( FA : UMA )  
 ( FF : DGPU = Nvidia MX130 +V2G )  
 ( FN : DGPU = Nvidia MX150 +V2G )

## Non Connected Standby

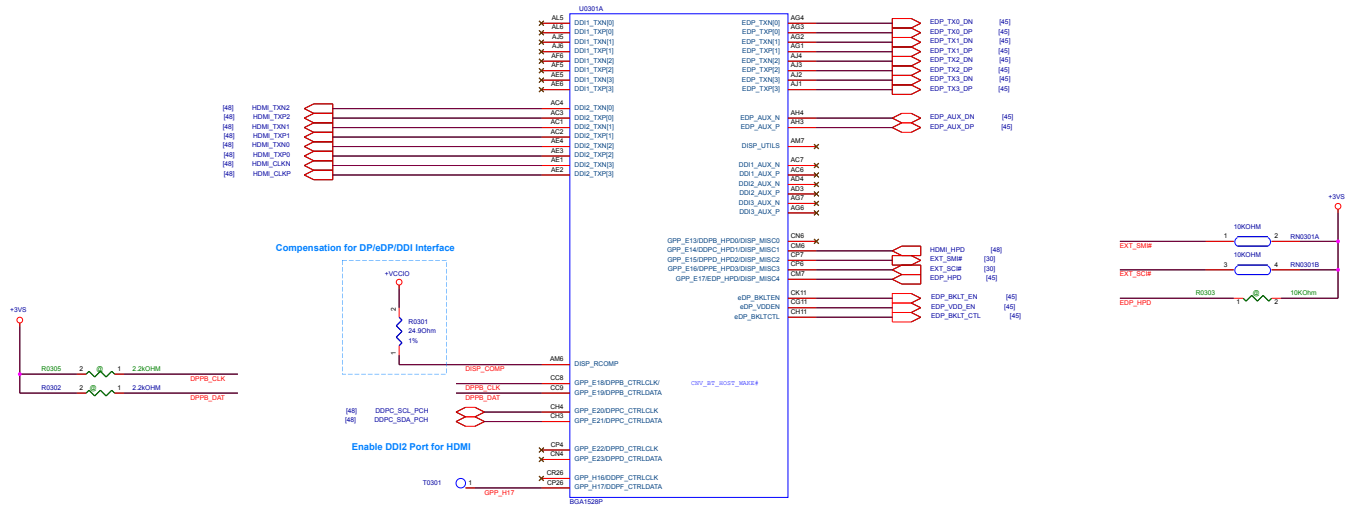


## Power



### Display Port

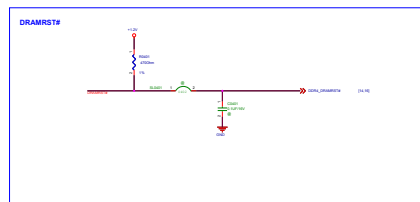
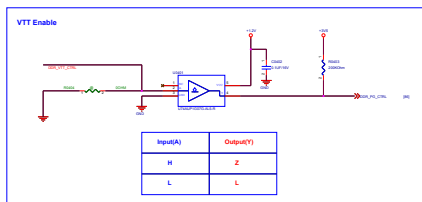
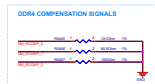
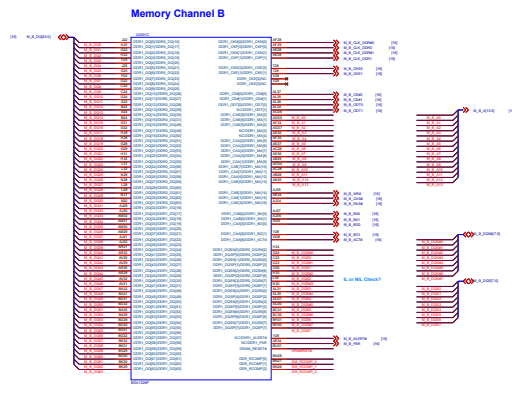
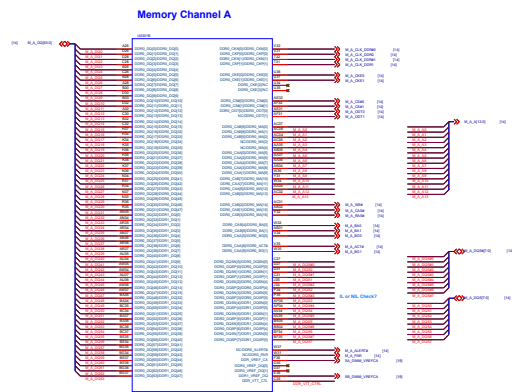
A	eDP
B	N/A
C	HDMI

DDI1 mapping DDPB  
DDI2 mapping DDPC

GPP_H17	Reserved	Rising edge of PCH_PWROK	<p>This signal has a weak internal pull-down. This strap should sample LOW. There should NOT be any on-board device driving it to opposite direction during strap sampling.</p> <p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>1. The internal pull-down is disabled after PCH_PWROK is high.</li> <li>2. This signal is in the primary well.</li> </ol>
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The diagram illustrates two types of interleave:

- Interleave back to back:** This diagram shows two interleaved data streams, Ch A and Ch B, each consisting of a sequence of data blocks (e.g., Ch A: 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9, 0xA, 0xB, 0xC, 0xD, 0xE, 0xF, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F, 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E, 0x6F, 0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77, 0x78, 0x79, 0x7A, 0x7B, 0x7C, 0x7D, 0x7E, 0x7F, 0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87, 0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F, 0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0, 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7, 0xA8, 0xA9, 0xAA, 0xAB, 0xAC, 0xAD, 0xAE, 0xAF, 0xB0, 0xB1, 0xB2, 0xB3, 0xB4, 0xB5, 0xB6, 0xB7, 0xB8, 0xB9, 0xBA, 0xBB, 0xBC, 0xBD, 0xBE, 0xBF, 0xC0, 0xC1, 0xC2, 0xC3, 0xC4, 0xC5, 0xC6, 0xC7, 0xC8, 0xC9, 0xCA, 0xCB, 0xCC, 0xCD, 0xCE, 0xCF, 0xD0, 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xD8, 0xD9, 0xDA, 0xDB, 0xDC, 0xDD, 0xDE, 0xDF, 0xE0, 0xE1, 0xE2, 0xE3, 0xE4, 0xE5, 0xE6, 0xE7, 0xE8, 0xE9, 0xEA, 0xEB, 0xEC, 0xED, 0xEE, 0xEF, 0xF0, 0xF1, 0xF2, 0xF3, 0xF4, 0xF5, 0xF6, 0xF7, 0xF8, 0xF9, 0xFA, 0xFB, 0xFC, 0xFD, 0xFE, 0xFF). The streams are interleaved such that the data from Ch A and Ch B are stored in a single, continuous sequence of blocks.
- Non-interleave side by side:** This diagram shows two interleaved data streams, Ch A and Ch B, each consisting of a sequence of data blocks (e.g., Ch A: 0x1, 0x2, 0x3, 0x4, 0x5, 0x6, 0x7, 0x8, 0x9, 0xA, 0xB, 0xC, 0xD, 0xE, 0xF, 0x10, 0x11, 0x12, 0x13, 0x14, 0x15, 0x16, 0x17, 0x18, 0x19, 0x1A, 0x1B, 0x1C, 0x1D, 0x1E, 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24, 0x25, 0x26, 0x27, 0x28, 0x29, 0x2A, 0x2B, 0x2C, 0x2D, 0x2E, 0x2F, 0x30, 0x31, 0x32, 0x33, 0x34, 0x35, 0x36, 0x37, 0x38, 0x39, 0x3A, 0x3B, 0x3C, 0x3D, 0x3E, 0x3F, 0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F, 0x50, 0x51, 0x52, 0x53, 0x54, 0x55, 0x56, 0x57, 0x58, 0x59, 0x5A, 0x5B, 0x5C, 0x5D, 0x5E, 0x5F, 0x60, 0x61, 0x62, 0x63, 0x64, 0x65, 0x66, 0x67, 0x68, 0x69, 0x6A, 0x6B, 0x6C, 0x6D, 0x6E, 0x6F, 0x70, 0x71, 0x72, 0x73, 0x74, 0x75, 0x76, 0x77, 0x78, 0x79, 0x7A, 0x7B, 0x7C, 0x7D, 0x7E, 0x7F, 0x80, 0x81, 0x82, 0x83, 0x84, 0x85, 0x86, 0x87, 0x88, 0x89, 0x8A, 0x8B, 0x8C, 0x8D, 0x8E, 0x8F, 0x90, 0x91, 0x92, 0x93, 0x94, 0x95, 0x96, 0x97, 0x98, 0x99, 0x9A, 0x9B, 0x9C, 0x9D, 0x9E, 0x9F, 0xA0, 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7, 0xA8, 0xA9, 0xAA, 0xAB, 0xAC, 0xAD, 0xAE, 0xAF, 0xB0, 0xB1, 0xB2, 0xB3, 0xB4, 0xB5, 0xB6, 0xB7, 0xB8, 0xB9, 0xBA, 0xBB, 0xBC, 0xBD, 0xBE, 0xBF, 0xC0, 0xC1, 0xC2, 0xC3, 0xC4, 0xC5, 0xC6, 0xC7, 0xC8, 0xC9, 0xCA, 0xCB, 0xCC, 0xCD, 0xCE, 0xCF, 0xD0, 0xD1, 0xD2, 0xD3, 0xD4, 0xD5, 0xD6, 0xD7, 0xD8, 0xD9, 0xDA, 0xDB, 0xDC, 0xDD, 0xDE, 0xDF, 0xE0, 0xE1, 0xE2, 0xE3, 0xE4, 0xE5, 0xE6, 0xE7, 0xE8, 0xE9, 0xEA, 0xEB, 0xEC, 0xED, 0xEE, 0xEF, 0xF0, 0xF1, 0xF2, 0xF3, 0xF4, 0xF5, 0xF6, 0xF7, 0xF8, 0xF9, 0xFA, 0xFB, 0xFC, 0xFD, 0xFE, 0xFF). The streams are interleaved such that the data from Ch A and Ch B are stored in separate, side-by-side sequences of blocks.

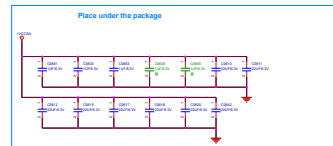
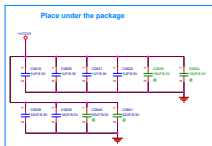
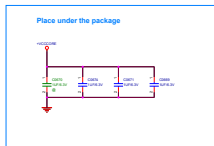
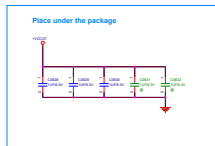
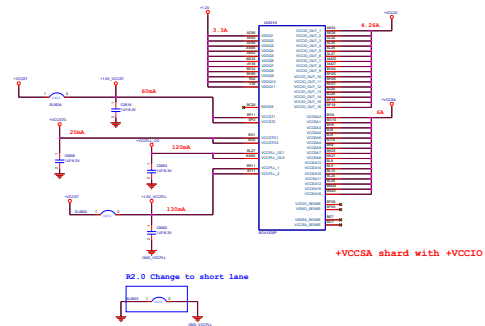
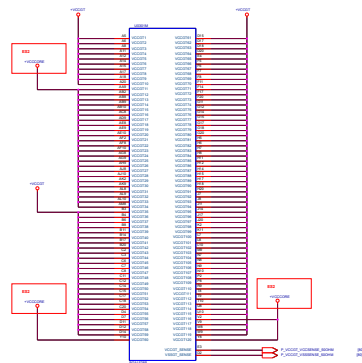
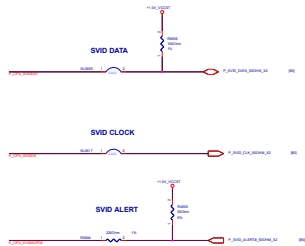
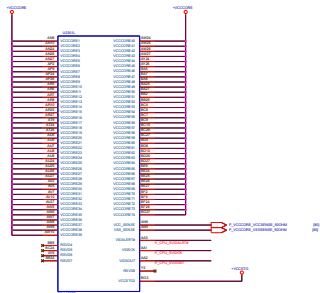


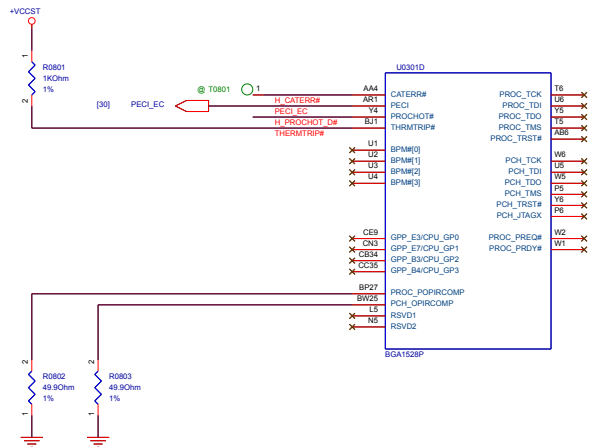
DDR4 SODIMM
DDR_RCOMP
DDR_RCOMP[0]: 125G ± 1% on pkg to VSS
DDR_RCOMP[1]: 80.6G ± 1% on pkg to VSS
DDR_RCOMP[2]: 100G ± 1% on pkg to VSS

[illegible]

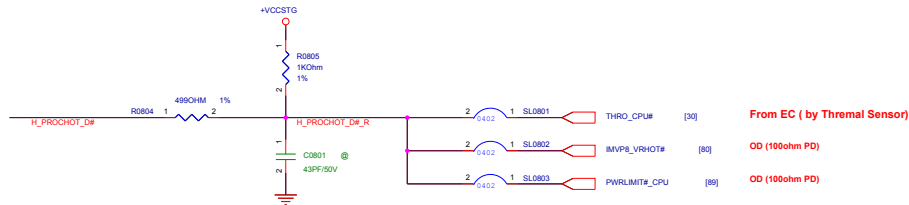
R1=470  
[5%]  
R2=0  
C1=0.1uF  
(no stuff)

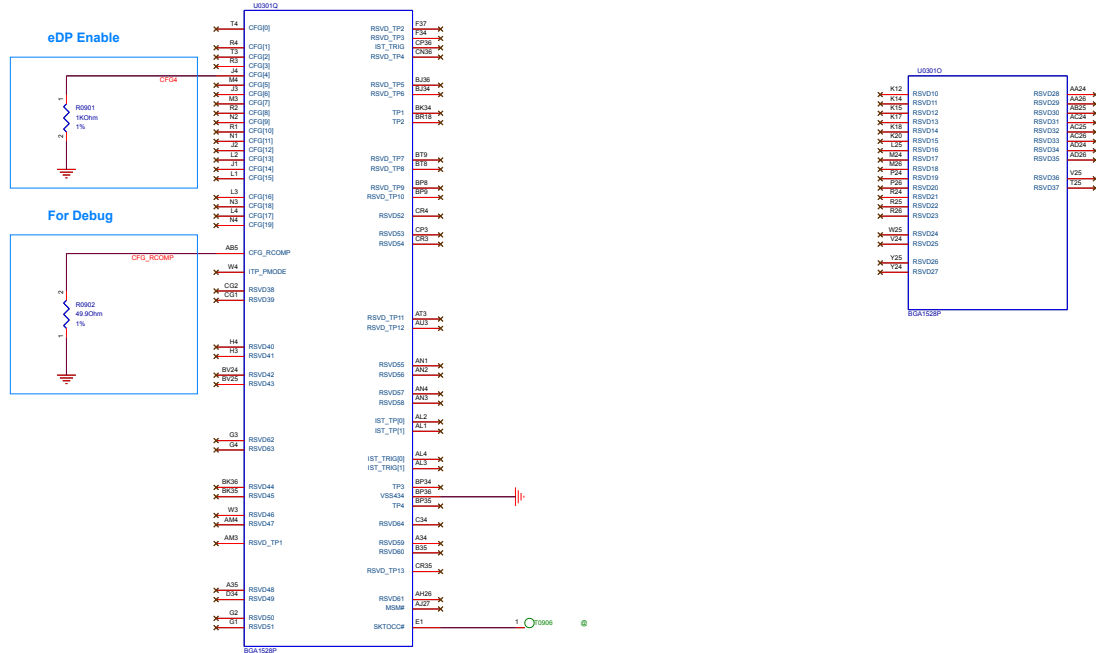


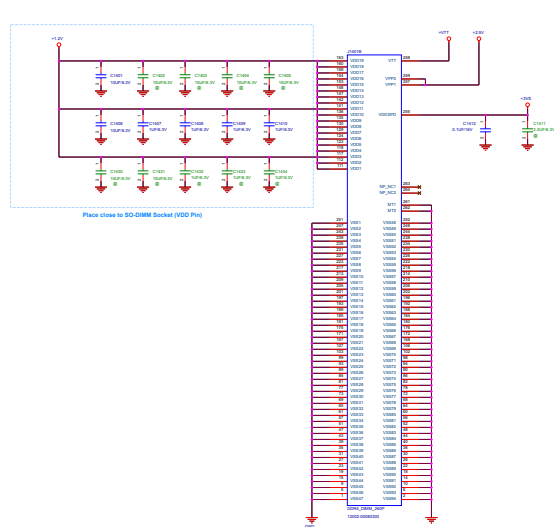
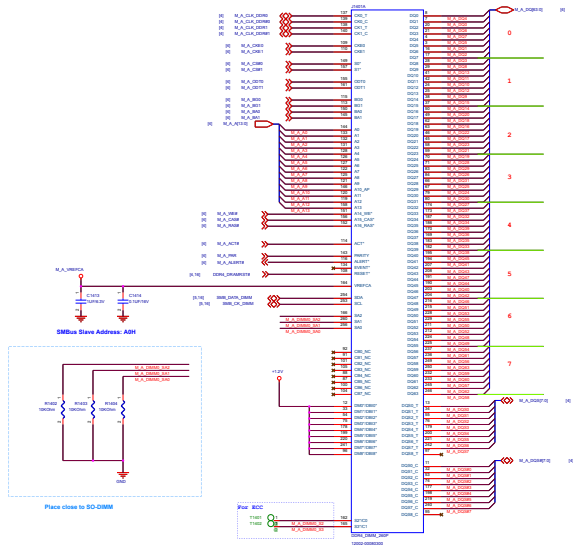




PU Power change from VCCIO to VCCSTG







Unused signals

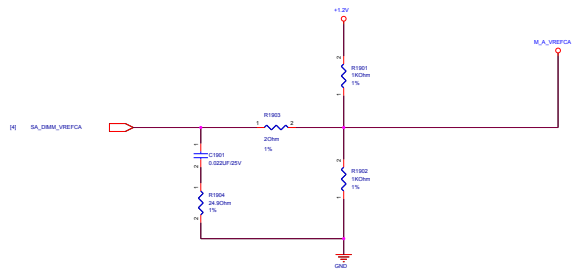
Connects to CPU and DIMM signals for testing through isolation resistor at SO-DIMM connectors, unless customer pin direction is not available, user is required to check.

Signal Name	Pin	Signal Name	Pin
AD0	1	AD1	2
AD2	3	AD3	4
AD4	5	AD5	6
AD6	7	AD7	8
AD8	9	AD9	10
AD10	11	AD11	12
AD12	13	AD13	14
AD14	15	AD15	16
AD16	17	AD17	18
AD18	19	AD19	20
AD20	21	AD21	22
AD22	23	AD23	24
AD24	25	AD25	26
AD26	27	AD27	28
AD28	29	AD29	30
AD30	31	AD31	32
AD32	33	AD33	34
AD34	35	AD35	36
AD36	37	AD37	38
AD38	39	AD39	40
AD40	41	AD41	42
AD42	43	AD43	44
AD44	45	AD45	46
AD46	47	AD47	48
AD48	49	AD49	50
AD50	51	AD51	52
AD52	53	AD53	54
AD54	55	AD55	56
AD56	57	AD57	58
AD58	59	AD59	60
AD60	61	AD61	62
AD62	63	AD63	64
AD64	65	AD65	66
AD66	67	AD67	68
AD68	69	AD69	70
AD70	71	AD71	72
AD72	73	AD73	74
AD74	75	AD75	76
AD76	77	AD77	78
AD78	79	AD79	80
AD80	81	AD81	82
AD82	83	AD83	84
AD84	85	AD85	86
AD86	87	AD87	88
AD88	89	AD89	90
AD90	91	AD91	92
AD92	93	AD93	94
AD94	95	AD95	96
AD96	97	AD97	98
AD98	99	AD99	100

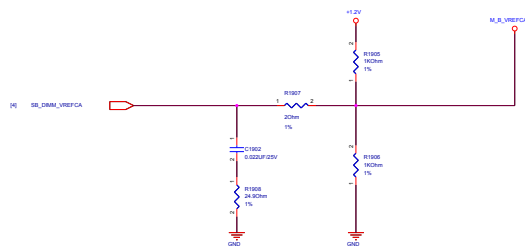




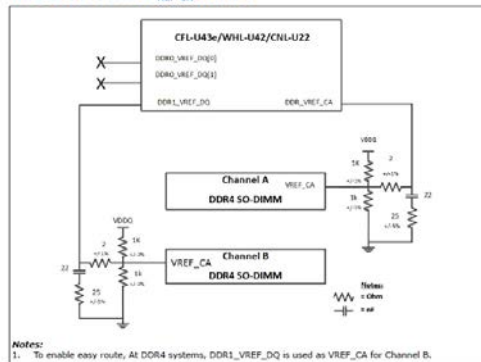
Close to SO-DIMM A



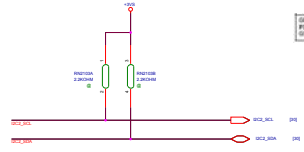
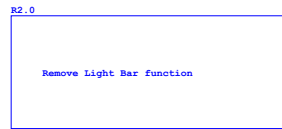
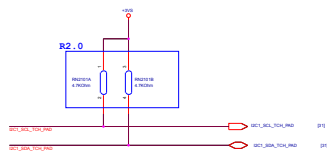
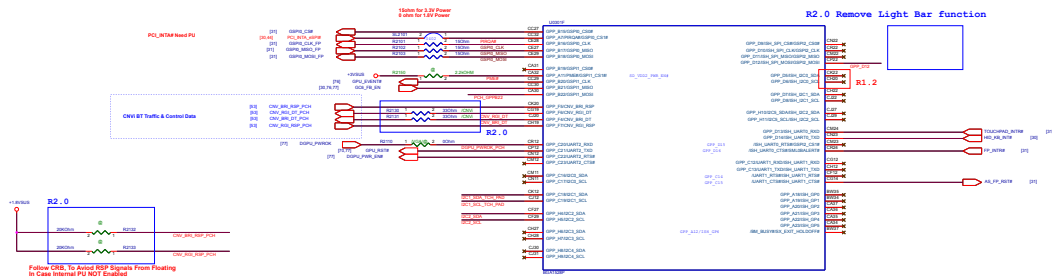
Close to SO-DIMM B



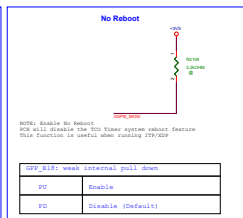
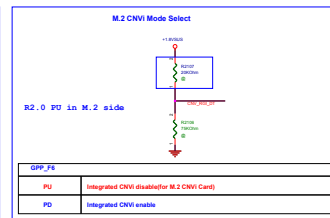
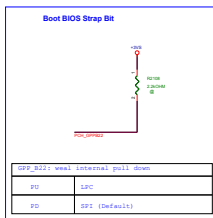
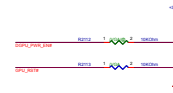
WHL U DDR4 SODIMM VREF-CA Overview







GPIO_A3 / PERIOA3 / GPIO_CS1*	I/O	PCI Interrupt Request A Note: An external Pull-up is required
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If during the first point above, if the CRF does not exist, the CNV\_RGI\_DT value will be driven by on-die or platform pull up resistors (typical 20K). In this case the strap will sample a logical High and the rest of the handshake process will not be performed.

## HD Audio

Place RN2281 near PCI

AC2\_BCLK\_ASD

AC2\_SYNC\_ASD

AC2\_SSP0\_ASD

AC2\_BSDOUT\_ASD

1

2

3

4

S20201A

S20201B

S20201C

S20201D

AC2\_BCLK\_ASD\_X1

AC2\_SYNC\_ASD\_X1

AC2\_SSP0\_ASD\_X1

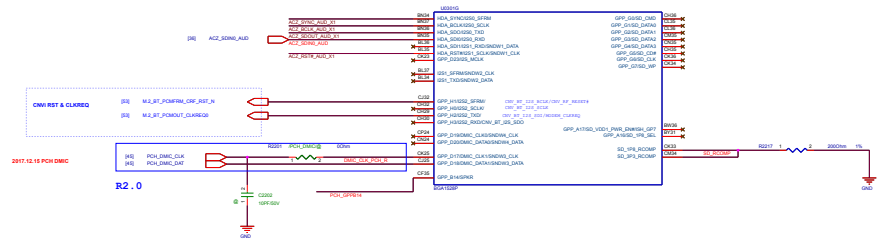
AC2\_BSDOUT\_ASD\_X1

BCLK\_ASD

10K

GND

RF requirement



This setup should only be asserted high using external Pull-up in manufacturing/Debug environments ONLY

Flash Descriptor Security Override	
RDA_SDO	weak internal pull down
PS	Disable Flash Descriptor Security (override)
PS	Enable security measures defined in the Flash Descriptor (Default)

Top Swap Override

PCW_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

PCE_GPPB14: weak internal pull down	
PU	Enable
PD	Disable (default)

PCIe Mapping Table

PCIe Controller 1#	1	USB1 PORT TYPE-A
	2	USB2.0 Port TYPE-C
	3	USB1 PORT TYPE-C
	4	N/A
PCIe Controller 2#	5	GPU X4 Lane0
	6	GPU X4 Lane1
	7	GPU X4 Lane2
	8	GPU X4 Lane3
	9	N/A
PCIe Controller 3#	10	WLAN BT
	11	WLAN_2SD
	12	N/A
PCIe Controller 4#	13	PCIE_M1_5SD_Lane0
	14	PCIE_M2_5SD_Lane0
	15	PCIE_M3_5SD_Lane0
	16	PCIE&SATA_M1_5SD_Lane0

Note: GPU X4 is in PCIe Controller 2#

USB Mapping Table

USB		USB	
1	USB2.0 Port	USB1_1	USB 3.0 Port (Type-A)
2	TYPE-C USB3.0 Port	USB1_2	USB 3.0 Port (Type-C)
3	IO USB2.0 Port1	USB1_3	N/A
4	IO USB2.0 Port2	USB1_4	N/A
5	Camera		
6	Card Reader		
7	USB TP		
8	BT		
9	Light Bar		
10	N/A		

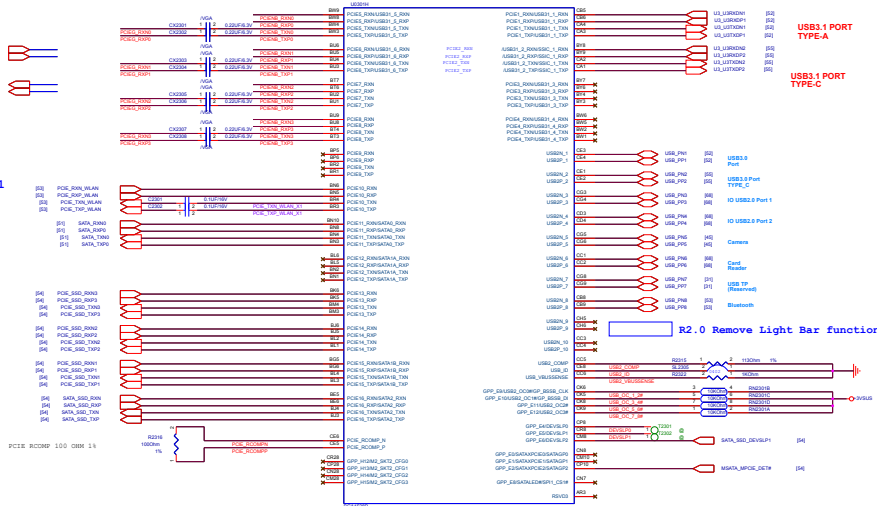
PCIeX4 GPU



PCIeX1 WLAN

SATA HDD

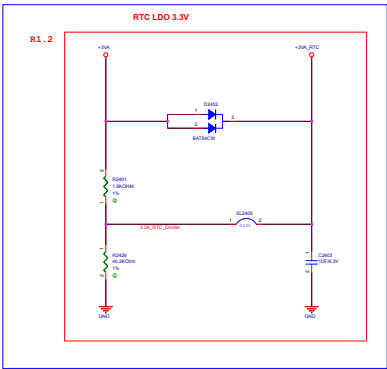
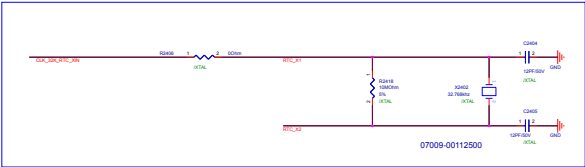
PCIeX4/SATAx1 SSD



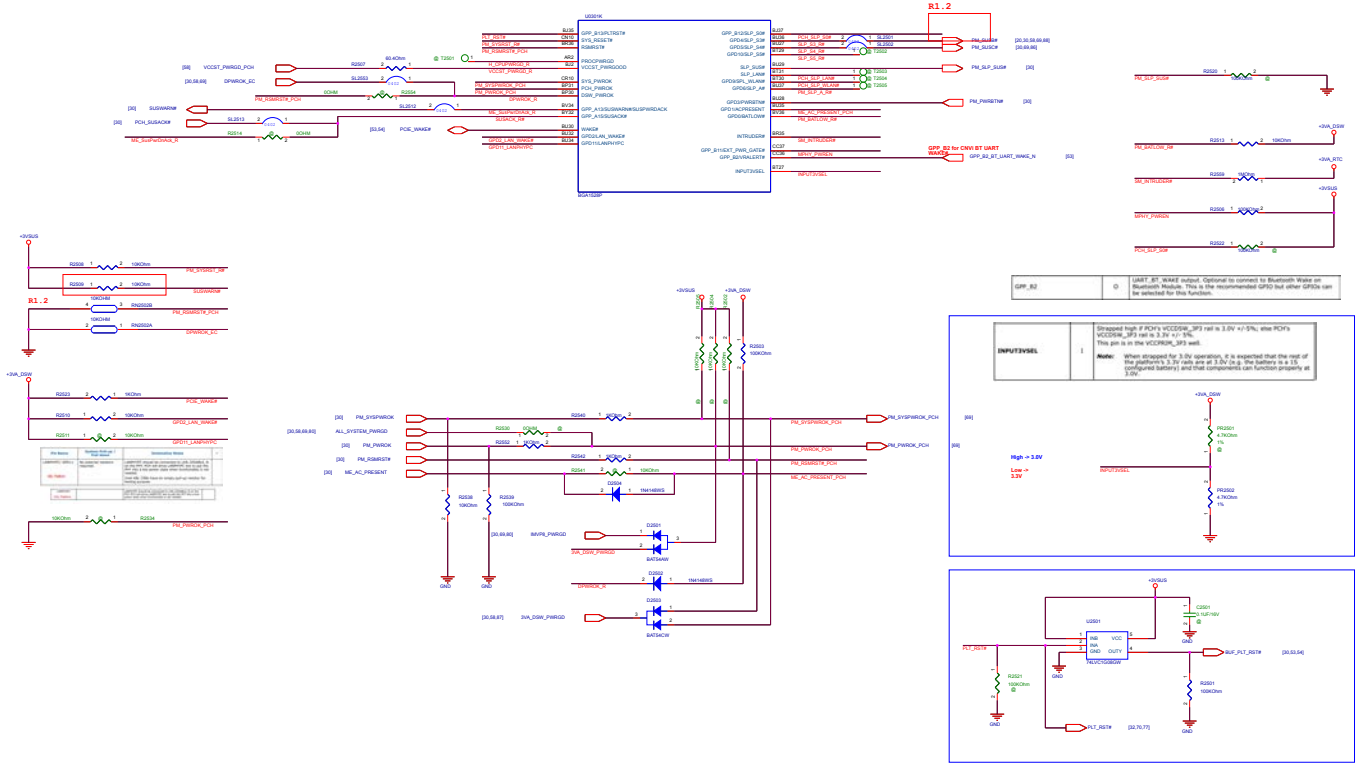
USB1.1 PORT TYPE-A

USB3.1 PORT TYPE-C

R2.0 Remove Light Bar function



# Main Board











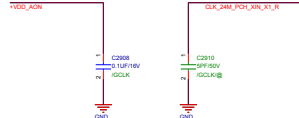
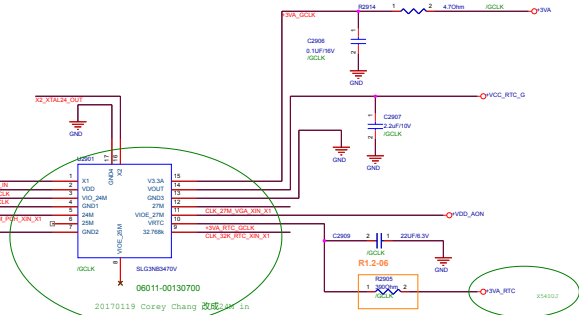
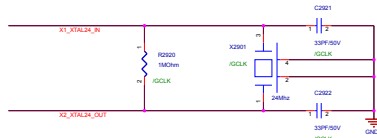
# Silego Green CLK

+3.3A power rail is always power under any mode

20180515 Corey COLAY +VCCIO and +1.0VBSU5

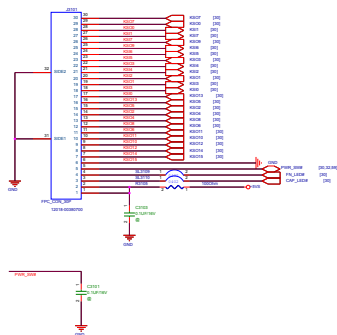
VDD must supply same power rail or prior to VDDIO\_25M\_A  
 & VDDIO\_25M\_B for Wake Function  
 VDDIO\_25M\_A MUST supply  
 same power rail as L3A\_3.3V  
 VDDIO\_25M\_B MUST supply  
 same power rail as PCR of XTALIN\_25M

U2901  
 N16 : 06011-00130700  
 N17 : 06011-00130900  
 R2906  
 N16 : 10G212220004010  
 N17 : 10G21210R014010

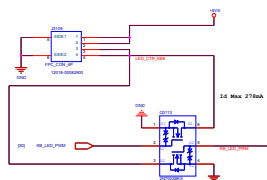




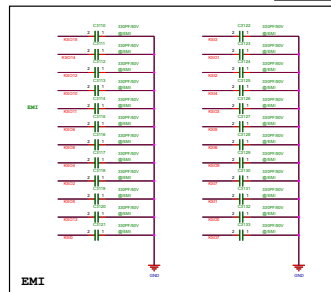
## Keyboard Connector



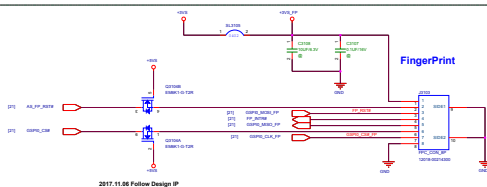
## light keyboard



## Main Board

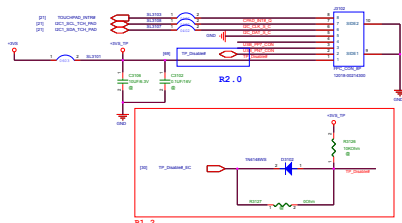


PIN NO.	PIN DEFINE*	PIN NO.	PIN DEFINE*
1	VDD_3.3V_TP	1	VDD_3.3V_FP
2	GND	2	FP_RSTN
3	PS2_CLK	3	FP_MOSI
4	PS2_DATA	4	FP_INTN
5	GND	5	FP_MISO
6	SDA	6	FP_CSN
7	SCL	7	FP_SCK
8	INT	8	GND



2017.11.06 Follow Design IP

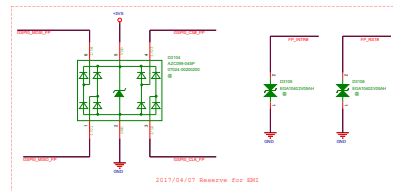
## TouchPad



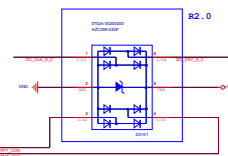
## USB Finger printer (Reserved)

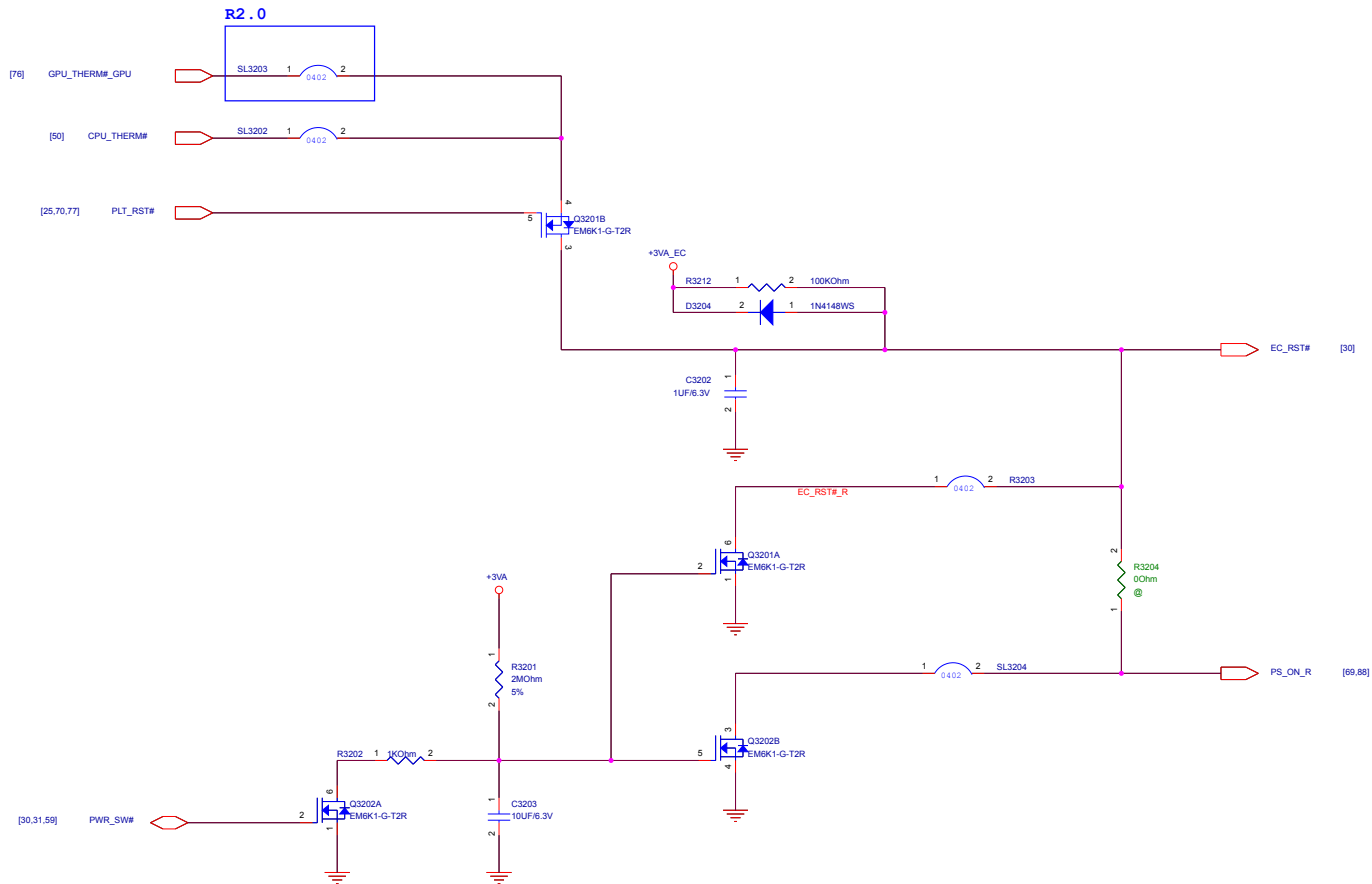
PIN NO.	PIN DEFINE*
1	VDD_3.3V
2	GND
3	FP_RSTN
4	FP_MOSI
5	FP_INTN
6	FP_CSN
7	FP_SCK
8	GND

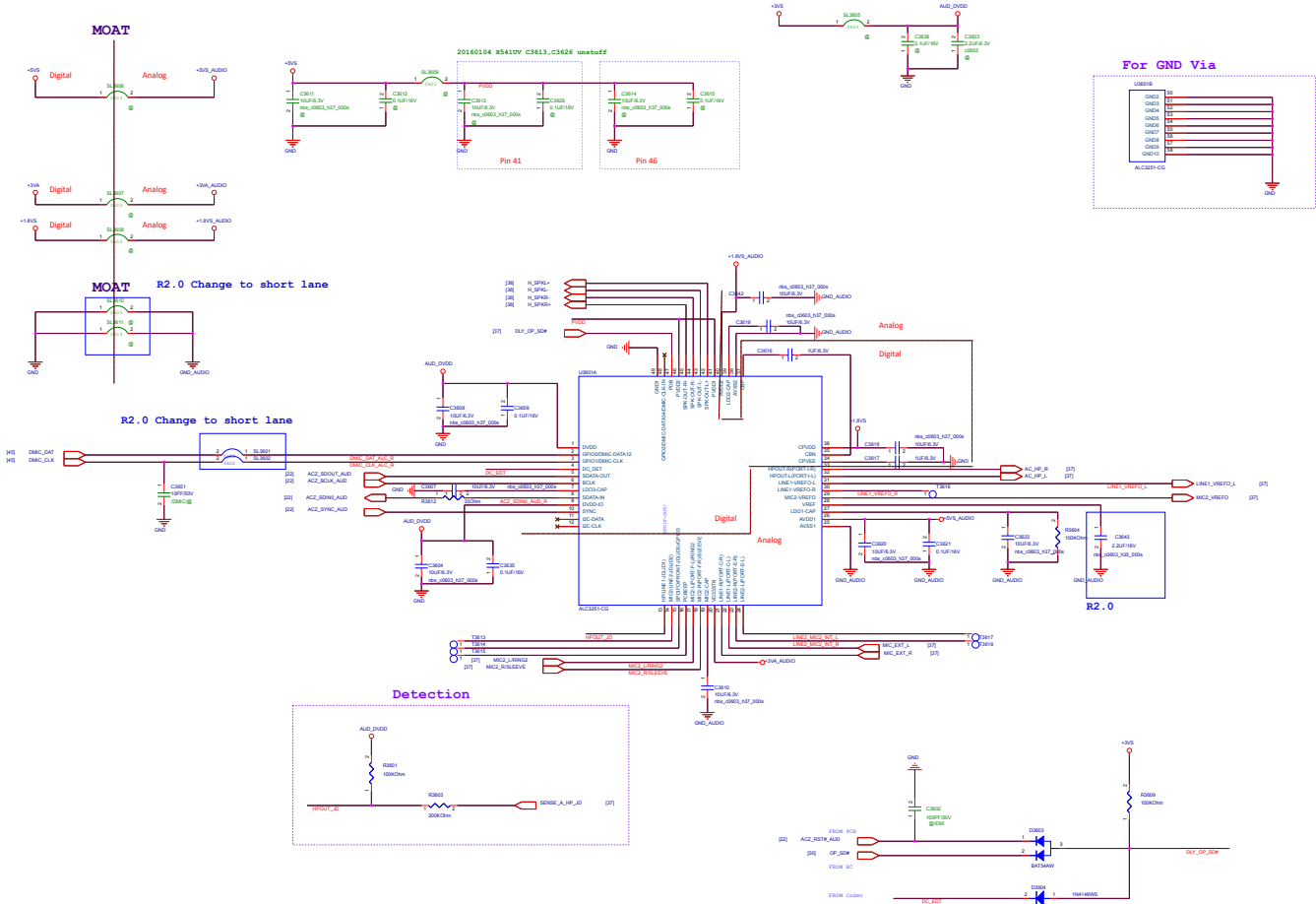
2017.11.06 Follow Design IP



2017/04/07 Reserve For EMI









81.3. Item 12.  
Add 4 pole handout jack normal  
open type for project demand.

- 尺寸：一部分三層規格，2.5mm、3.5mm、6.35mm，
- 種類：一部分三層規格，TE 端子 (Micro)，TFS 端子 (Starco)，TFS 端子 (Starco + Mic/Videa)，

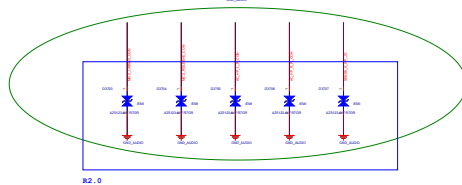


**CITA: 國際標準**  
 Series: 420000/NTC/中國 第 420000-Jack 國際

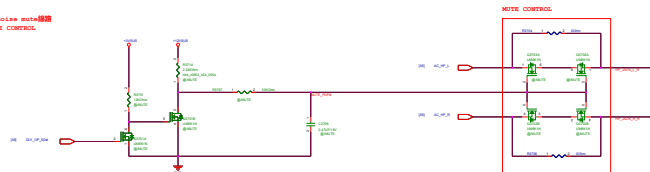
Apple	iPhone (WTC/00K)	iPhone 2nd ed 000		
Apple	iPad (Steno)	iPod (Steno)	Phone (Mc)	iPod (AV)
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	Right channel	Right channel	Right channel	Right channel
3. Ring1	-	-	Ground	Ground
4. Sleeve	Ground	Ground	Mc	Video

CECP: 國家標準

Standard	Mono	Stereo	Stereo + Mic	Audio + Video
1. Tip	Left channel	Left channel	Left channel	Left channel
2. Ring1	-	Right channel	Right channel	Video
3. Ring1	-	-	Mic	Ground
4. Sleeve	Ground	Ground	Ground	Right channel

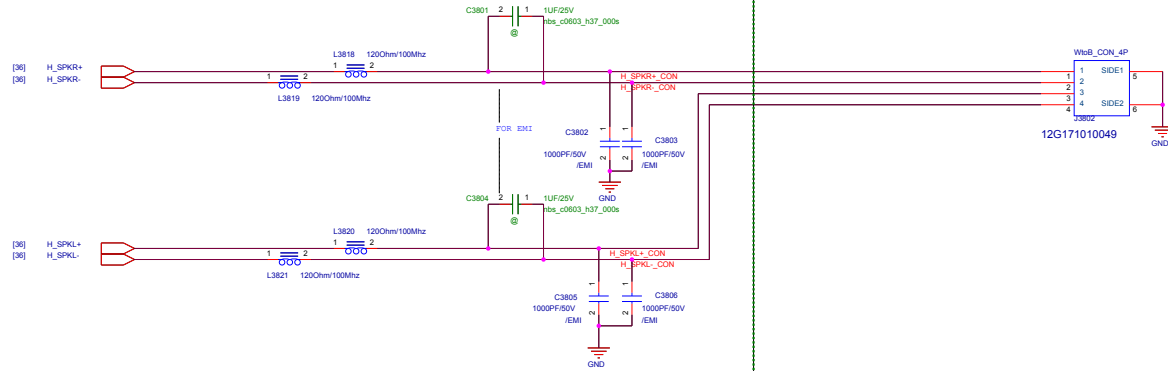


耳機pop noise mute線路  
MUTE CONTROL

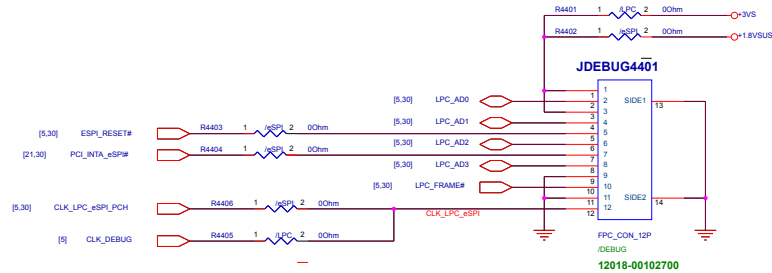


MUTE CONTROL

Trace width for  
H\_SPKL+\_O/H\_SPKL-\_O/H\_SPKR+\_O/H\_SPKR-\_OSpeaker  
Speaker : 4 ohm : 40mil ; 8 ohm : 20mil

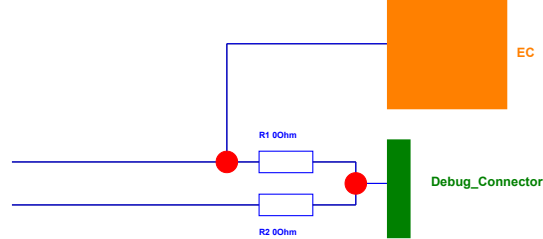


## LPC Debug Port



CLKOUT\_LPC0/ESPI\_CLK

CLKOUT\_LPC1



When in LPC Mode, LPC 0 & 1 are independent LPC Clock Source ->

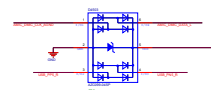
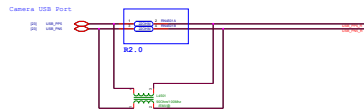
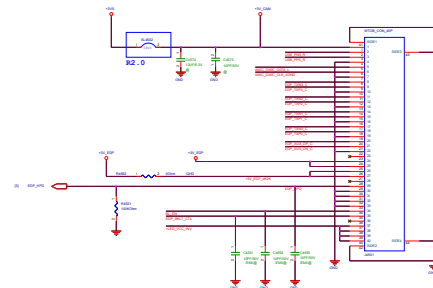
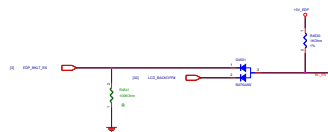
Stuff R2 and unstuff R1

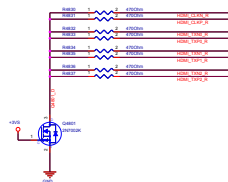
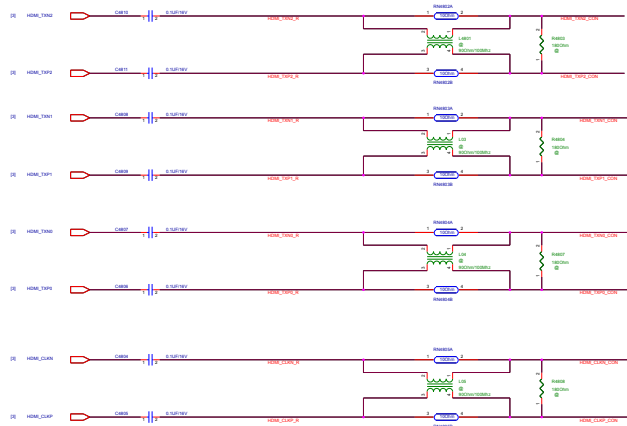
When in eSPI Mode, if LPC 0 & 1 are independent eSPI Clock Source ->

Stuff R2 and unstuff R1

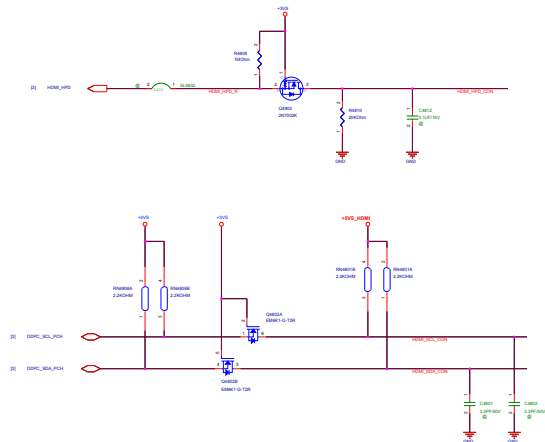
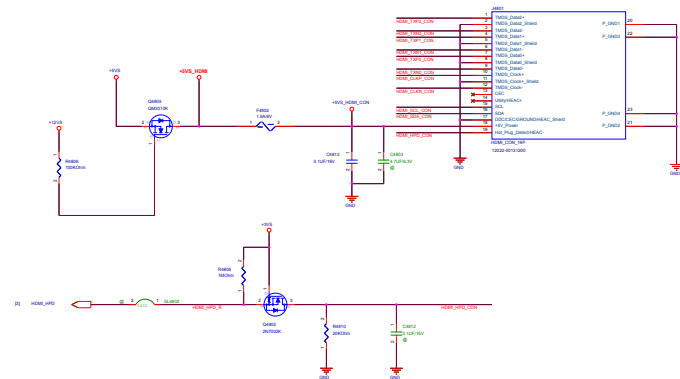
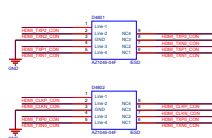
When in eSPI Mode, if LPC 0 is eSPI Clock and LPC 1 NO Output ->

Stuff R1 and unstuff R2





## ESD Protection



[illegible]

**CPU/PCB Board Thermal Sensor**

SMBus address=101000h (h)

**R2.0**  
Change part number

Set to 100°C

CPU\_THRM\_DA CPU\_THRM\_DC CPU\_THRM\_DG CPU\_THRM\_DP

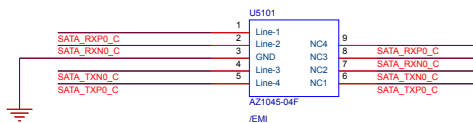
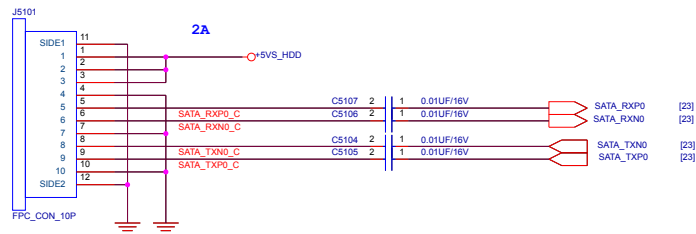
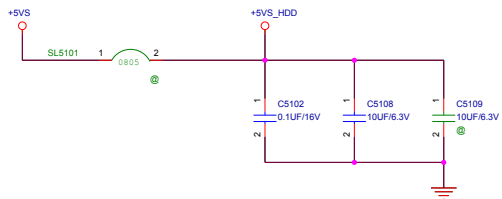
5.3 Address Setting  
NCT7717U I2C/SMBus address is 101000h (h is RW bit).

5.6 ALERT# pin hardware power-on setting (TBD)  
The default value could be set after power up 100ms by different pull-up resistor of ALERT# pin:

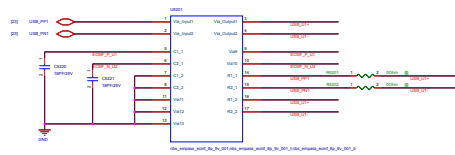
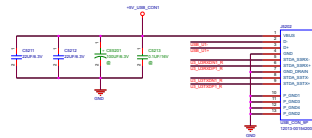
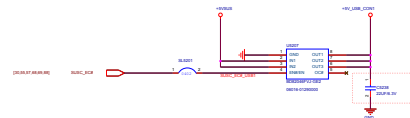
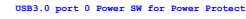
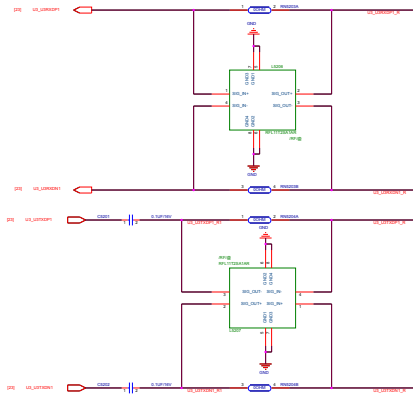
PULL-UP RESISTOR	TEMPERATURE (°C)
2KΩ	75
7.5KΩ	90
10.1KΩ	100
15KΩ	105
18.7KΩ	110

Route CPU\_THRM\_DA, CPU\_THRM\_DC and on the same layer

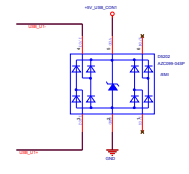
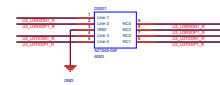
10 mils  
align=center=END  
10 mils  
align=right,THERM\_DA(10 mils)  
10 mils  
align=right,THERM\_DC(10 mils)  
10 mils  
align=right=END  
10 mils  
align=right=END  
Avoid FB3 Power



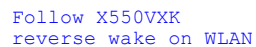
## USB3.0\_Port 0

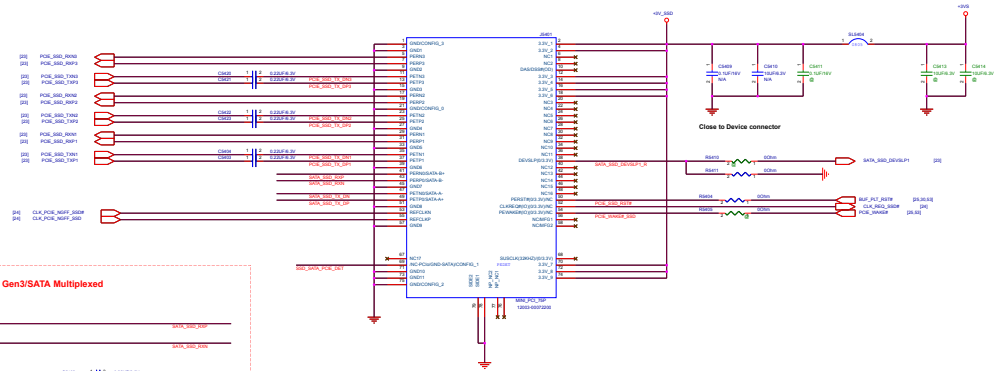


### ESD-Protection



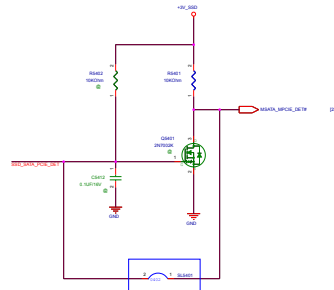




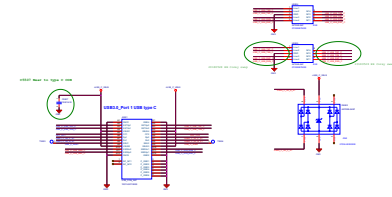
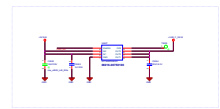
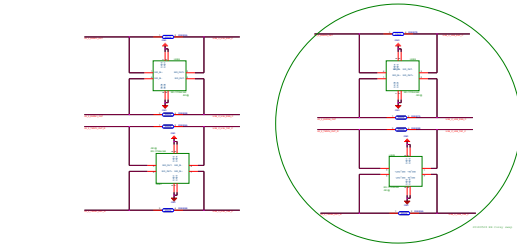
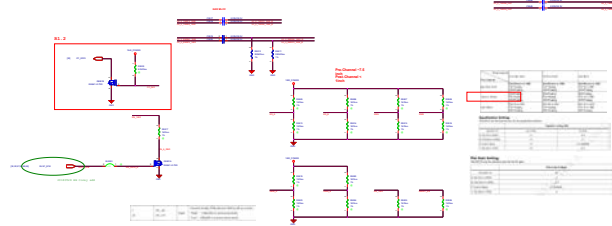
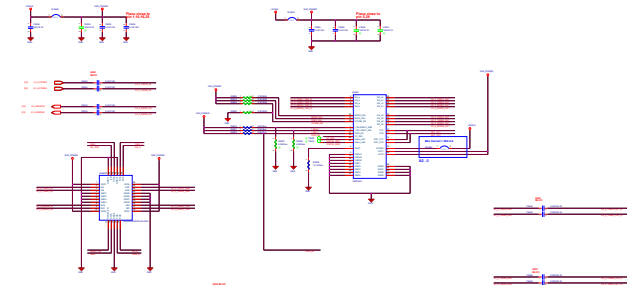


#### For PCIe/SATA Auto Detect

M.2 SSD Pin Define  
PCIe / SATA / GND

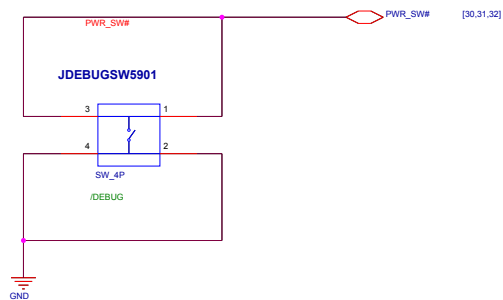
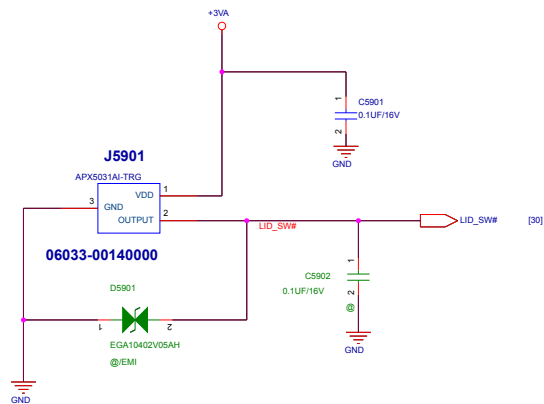


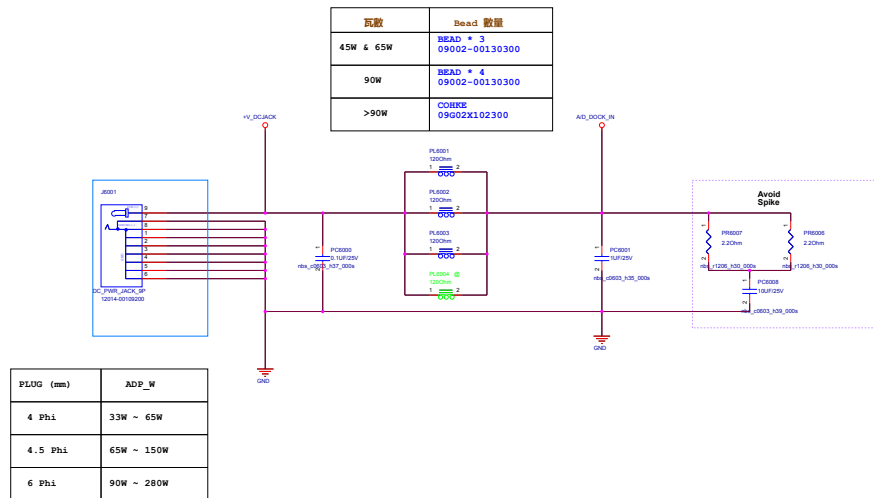
R2.0 Change to short lane



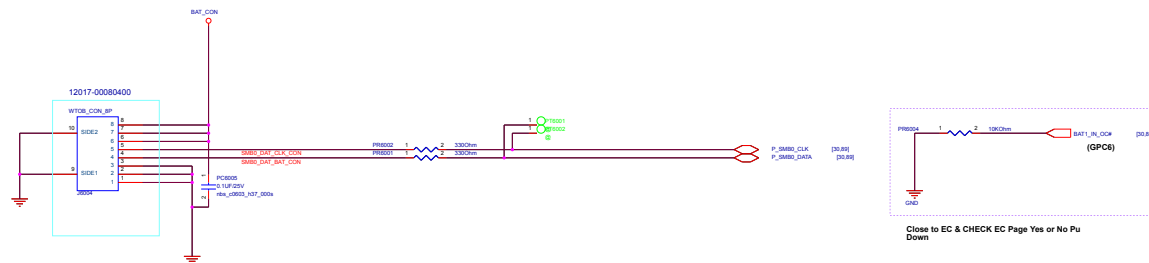


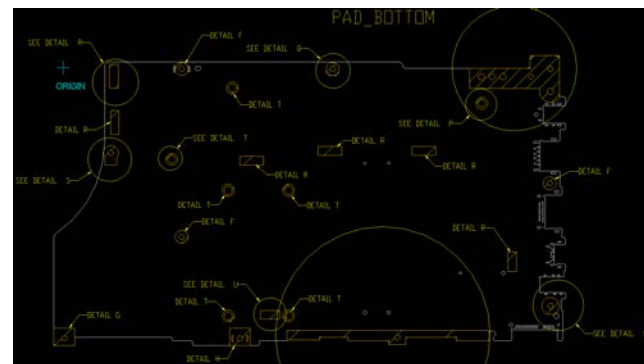
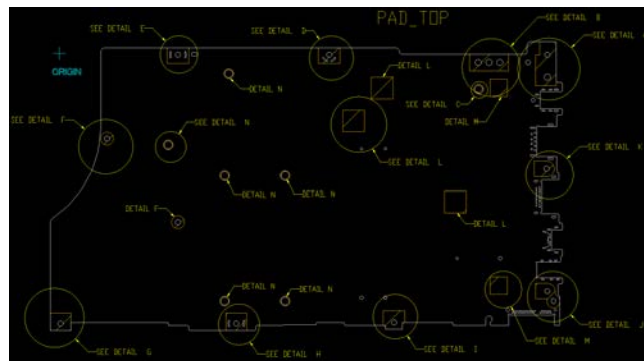
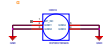
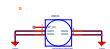
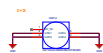
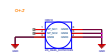
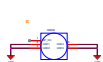
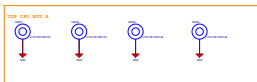




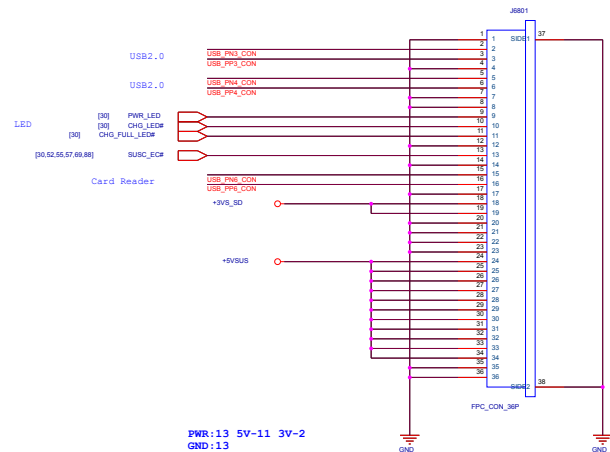


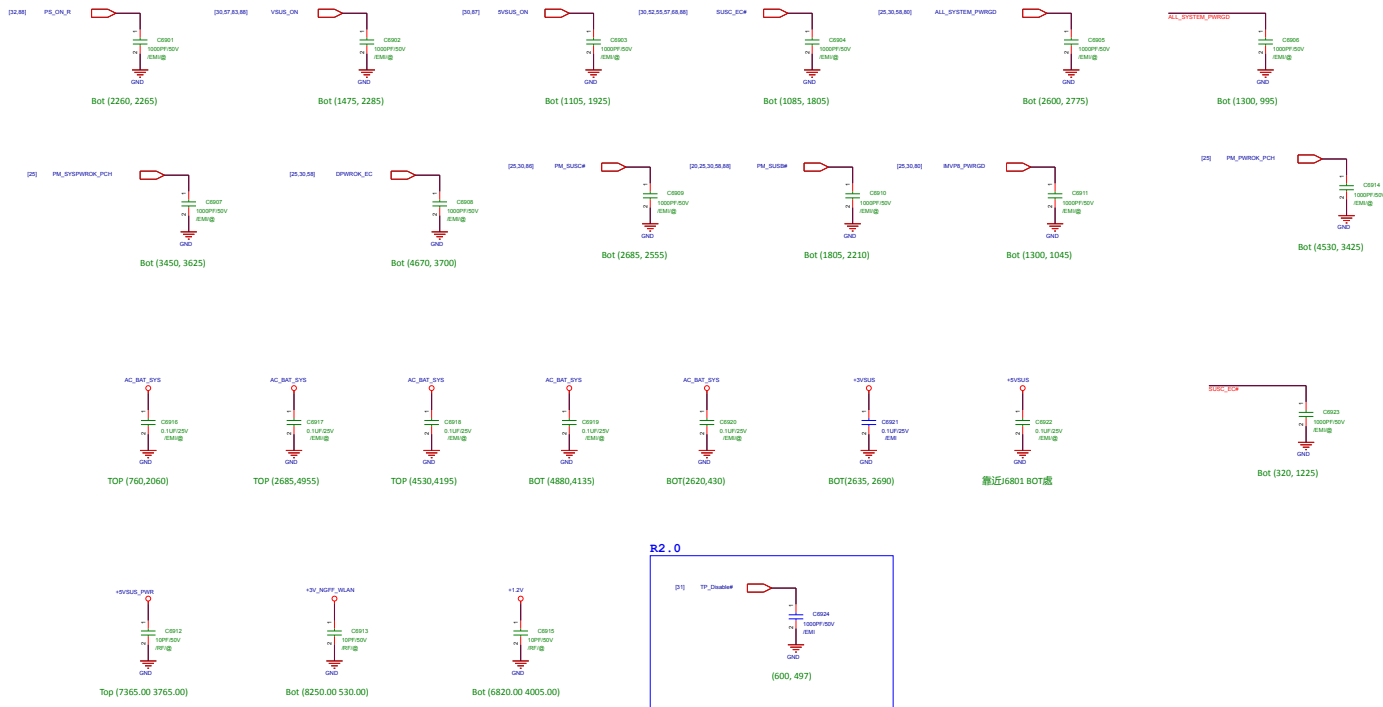
## Battery Connector



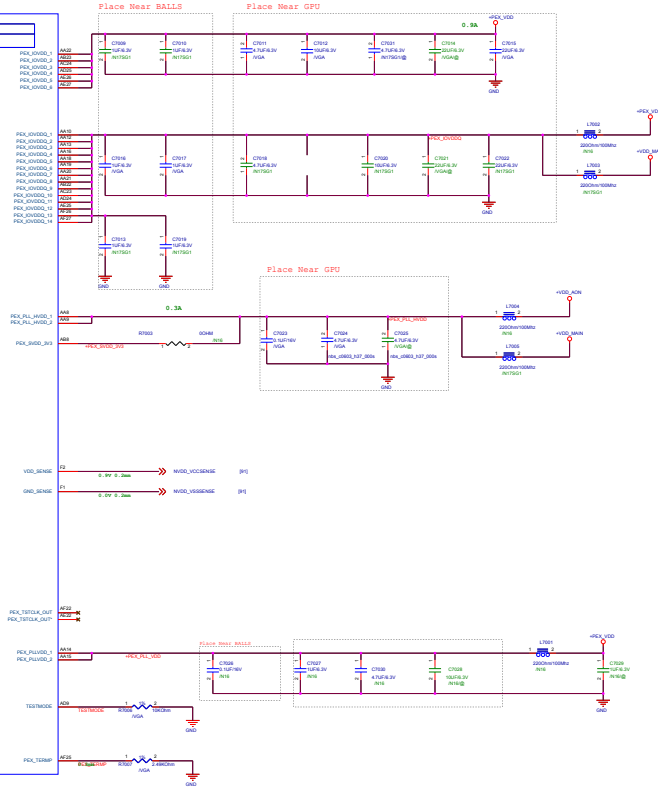
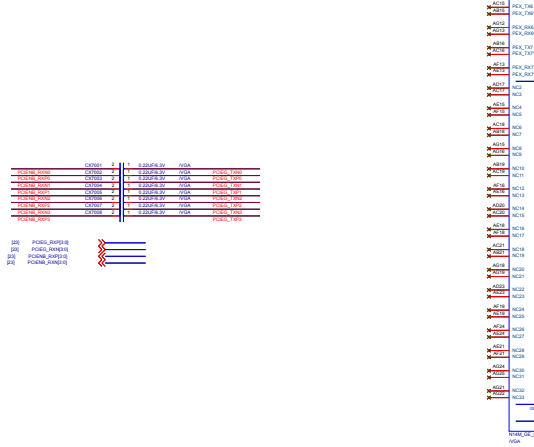
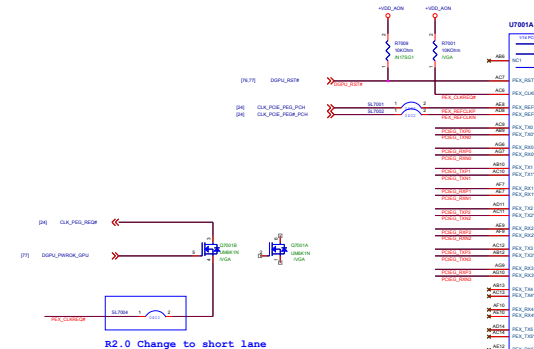
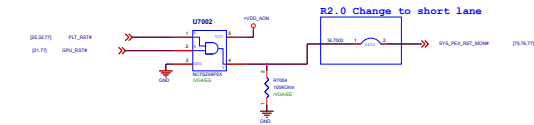


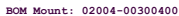






電容不要放Y5V

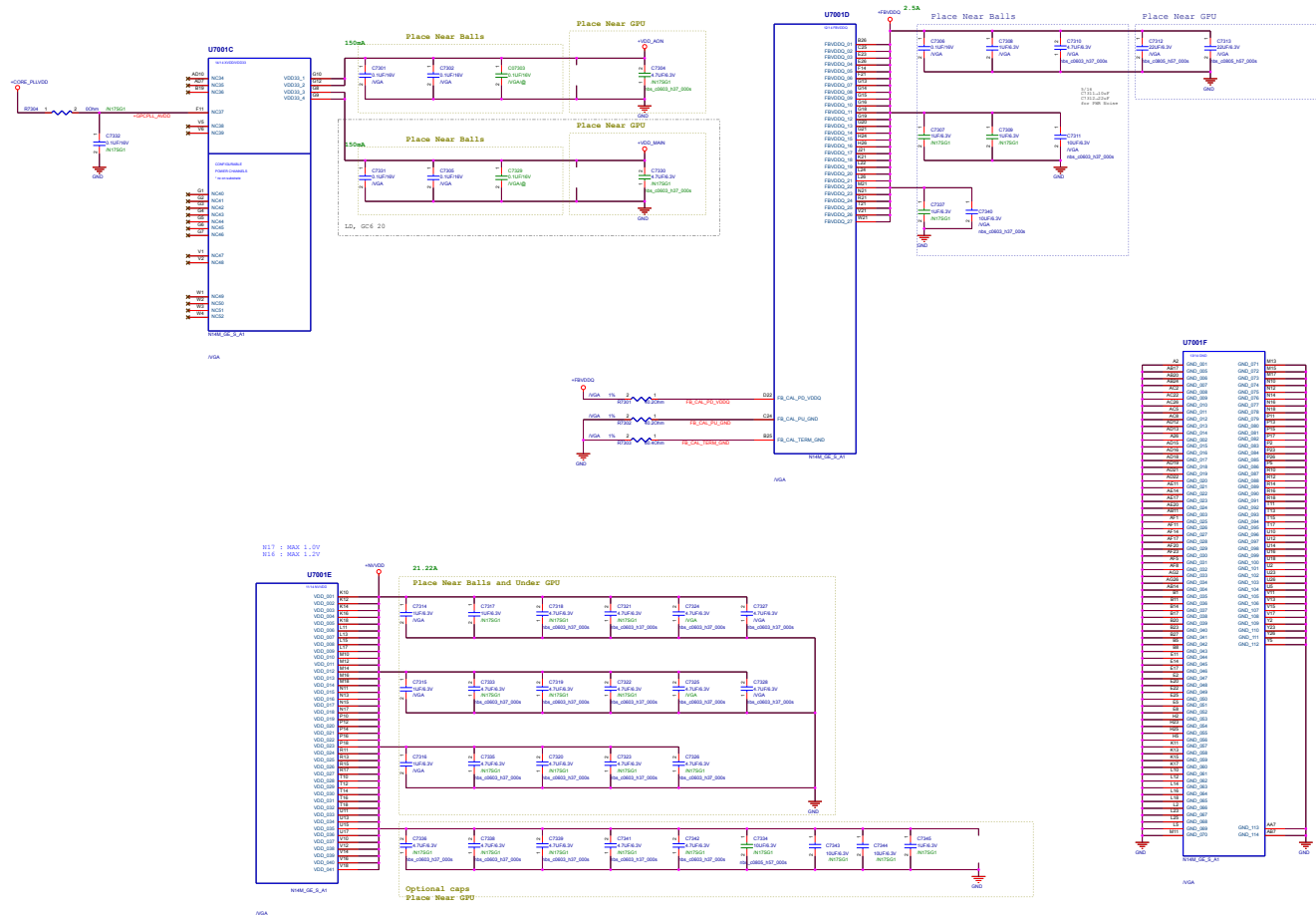




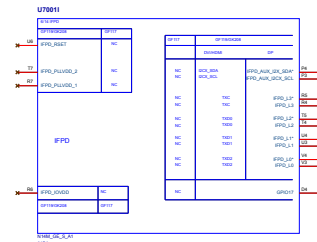
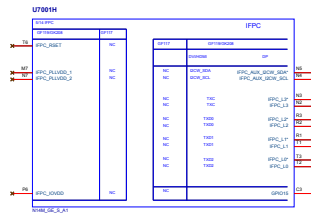
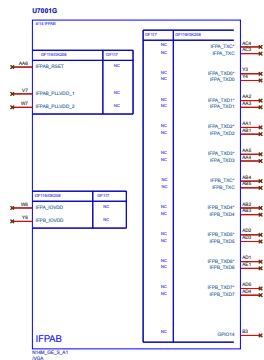
Note:

- GB2-64 32-bit implementation will use channel 1 data bits [63:32]. Unused channel data bits [31:0] can be left unconnected.
- For 32-bit implementation on GB2-64, please inform account AE for VBIOS support.

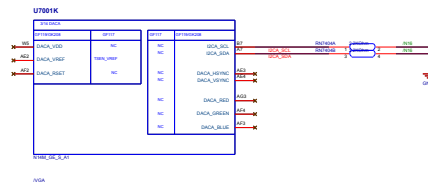
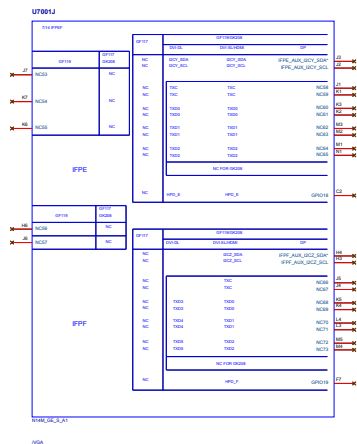




LVDS

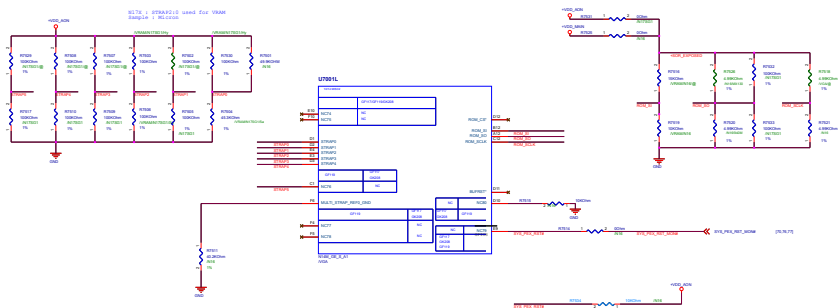


CRT

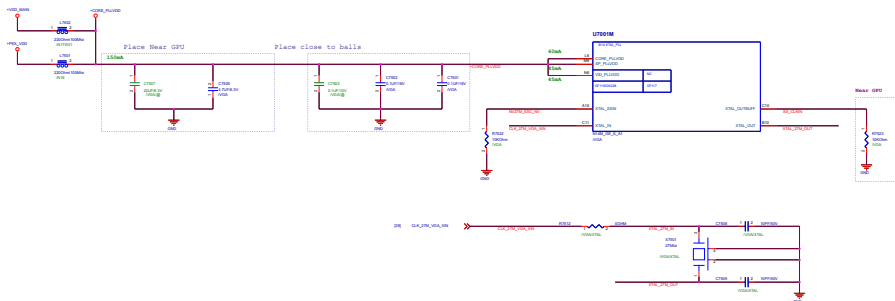


Stage Pins and Role			Reset PS Setting Number	
STRAP2	STRAP1	STRAP0	use arbitrary bit, for memory config (corresponding to these numbers)	
L	L	N	0 (0x0000)	M17/SAMSUNG
L	L	M	1 (0x0001)	
L	M	L	2 (0x0002)	
L	M	M	3 (0x0003)	
M	L	L	4 (0x0004)	M17/RTXIX
M	L	M	5 (0x0005)	
M	M	L	6 (0x0006)	
M	M	M	7 (0x0007)	
L	L	N	8 (0x0008)	M17/RTXIX
L	L	M	9 (0x0009)	
L	M	L	10 (0x000A)	
L	M	M	11 (0x000B)	
M	L	L	12 (0x000C)	M17/RTXIX
M	L	M	13 (0x000D)	

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



Xtal

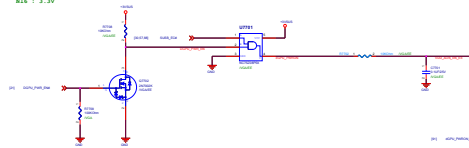




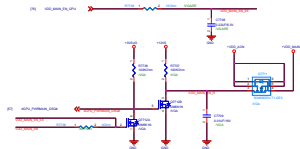
[illegible][illegible][illegible][illegible]

## dGPU Power Sequence

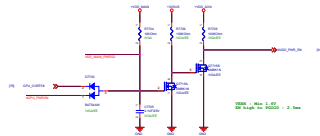
1. +VDD\_AIN  
M13 = 1.2V  
M16 = 3.2V



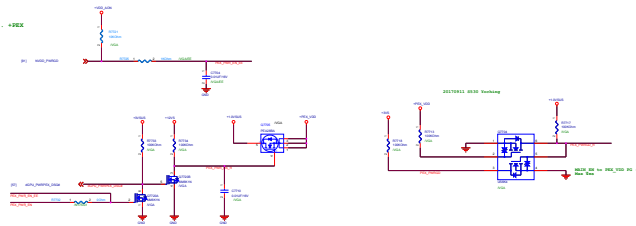
2. +VDD\_MAIN



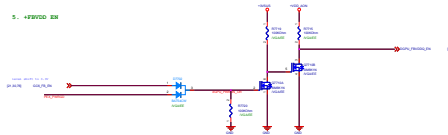
3. +VDDO\_EN



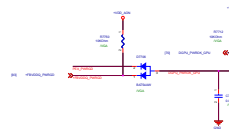
4. +PES



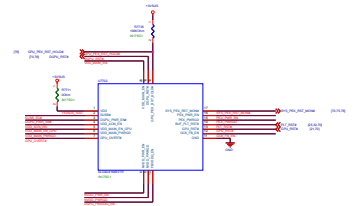
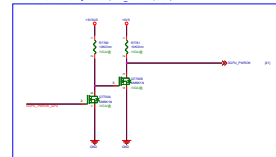
5. +PESVDDO\_EN



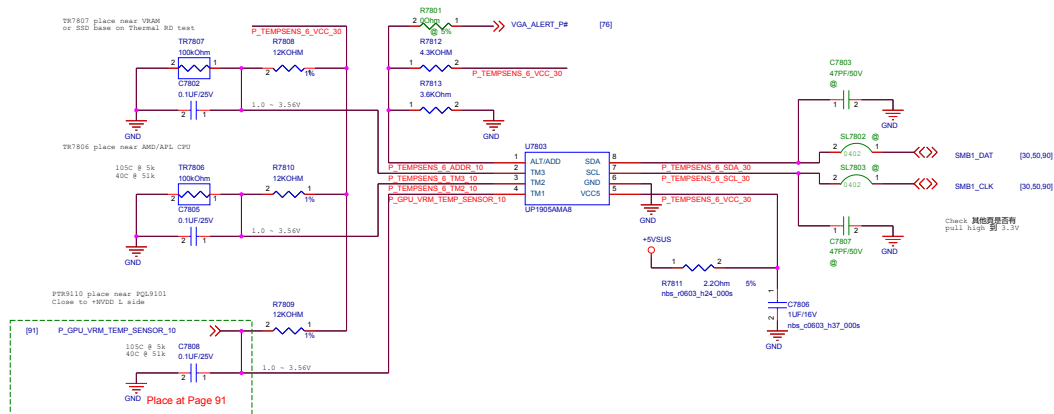
6. GPU POWER GOOD

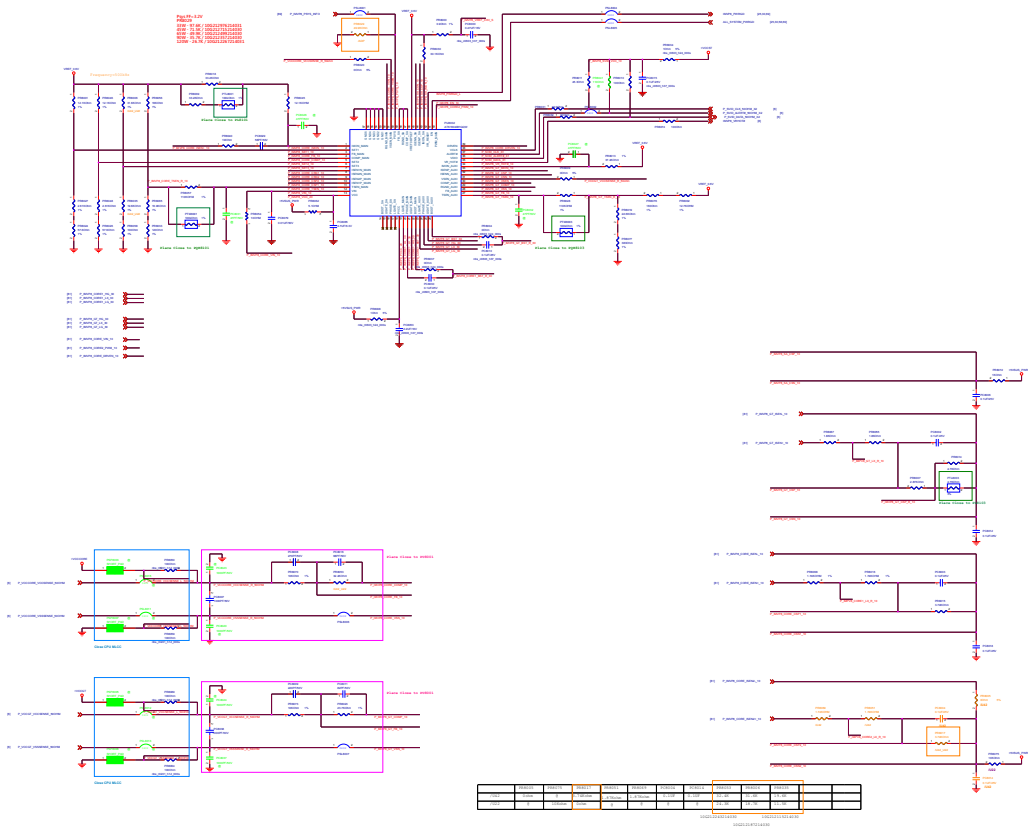


Level shifter for SPI power (M13, M16, M17, M18)



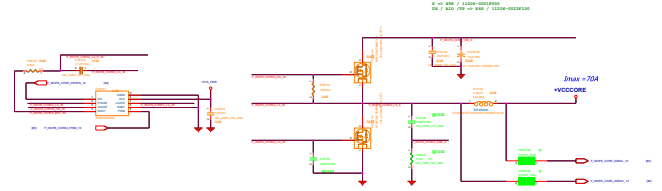
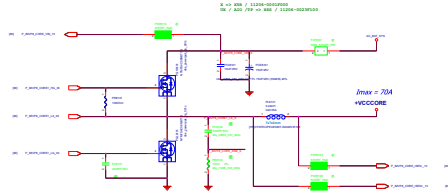
Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
R7812	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
R7813	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k



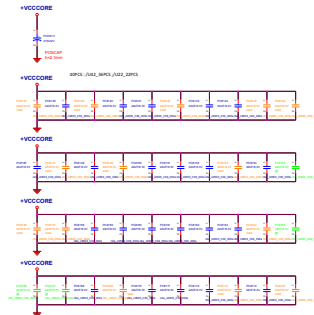
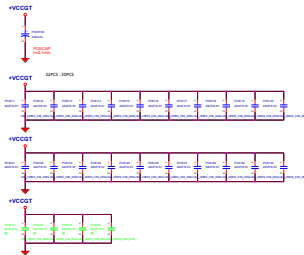
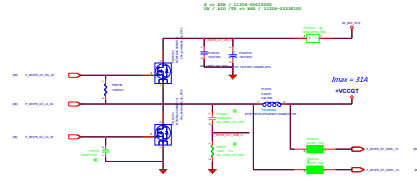


# Whisky LAKE IMVP8 Power (2)[For CPU]

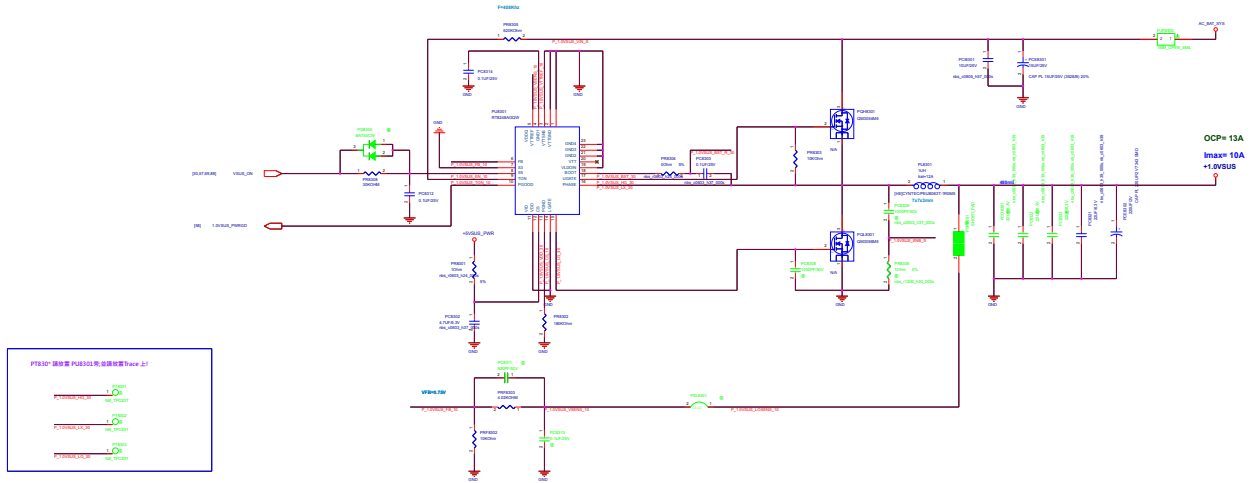
+VCCCORE



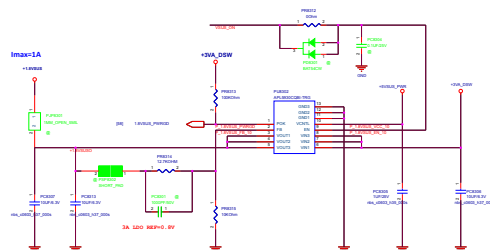
+VCCGT



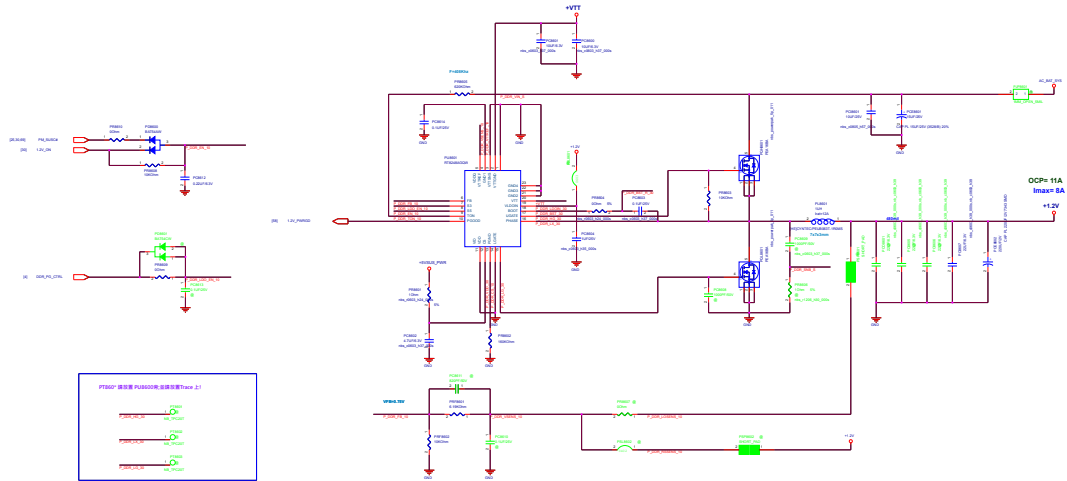
# +1.0VSUS [For PCH]



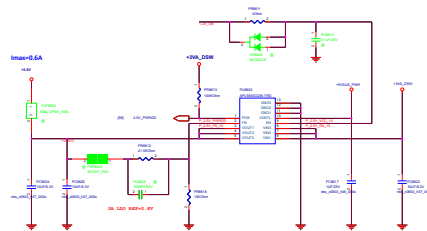
# +1.8VSUS [For PCH]



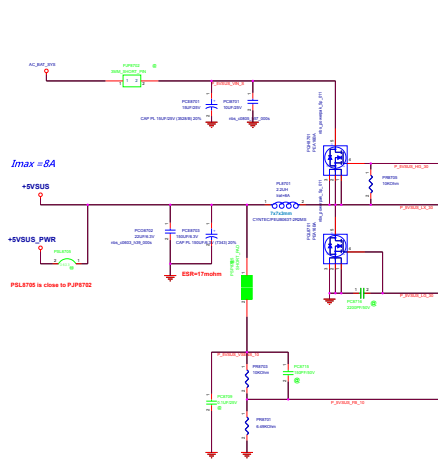
# +1.2V / +VTT[For Memory]



# +2.5V[For Memory]



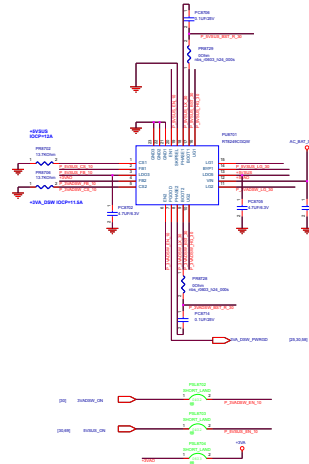
+3VA\_DSW / +5VSUS [System Power]



$I_{max} = 8A$

+5VSUS\_PWR

PSLE700 is close to P-MOSFET



SW

SW

Adaptor Mode (SWPS)

	SW	CS	SW	CS	SW	CS
P12_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
1.2V_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1

Battery Mode (SWPS)

	SW	CS	SW	CS	SW	CS
P12_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
1.2V_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1
SWPSW_0N	1	1	1	1	1	1

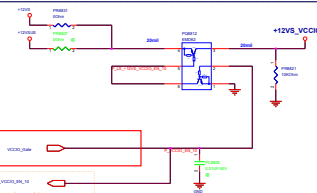
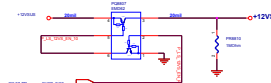
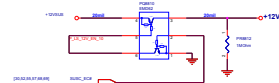
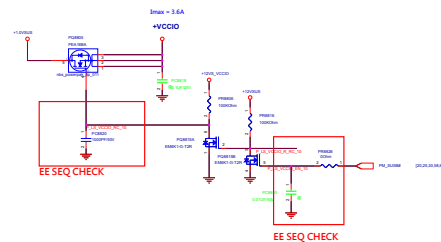
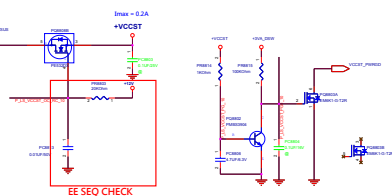
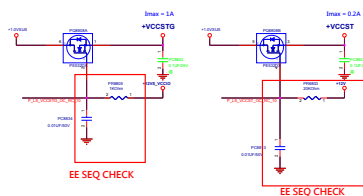
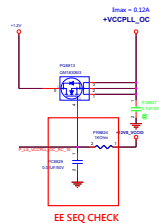
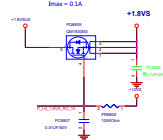
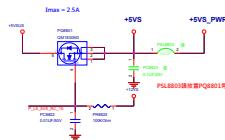
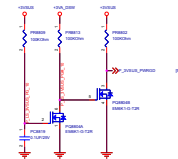
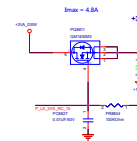
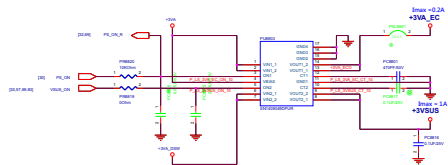
P12070 請注意 P12070 與 P12070 的連接位置



請 check 整個電路 +12VSUS total 電壓對地電壓不得小於1400mV



# Load Switch

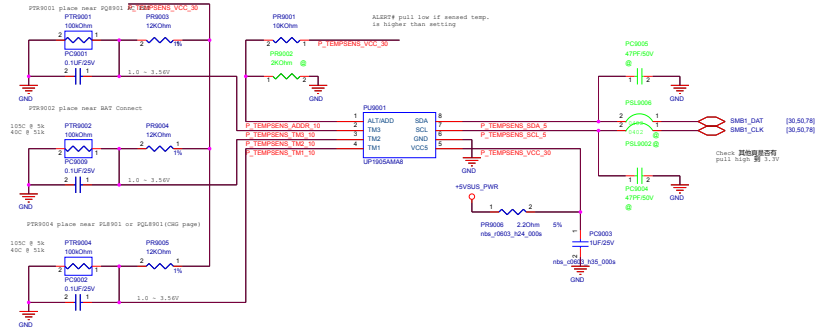


EE Add discharge circuit



Address	0x7E	0x7C	0x7A	0x78	0x76	0x74	0x72	0x70
PR0001	10k	1.5k	2k	3.6k	3.9k	4.3k	5.1k	6k
PR0002	Open	8.2k	6.2k	6.8k	4.7k	3.6k	2.7k	2k

Address	0x00	0x01	0x02	0x03	0x04	0x05	0x06
R/W	W	W	W	R	R	R	R
Function	Temp. alert threshold setting			Sensed temp. data			bit 4 = 0 bit 5 = 0 bit 6 = 0 When ALERT# assert

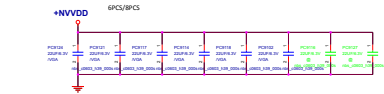
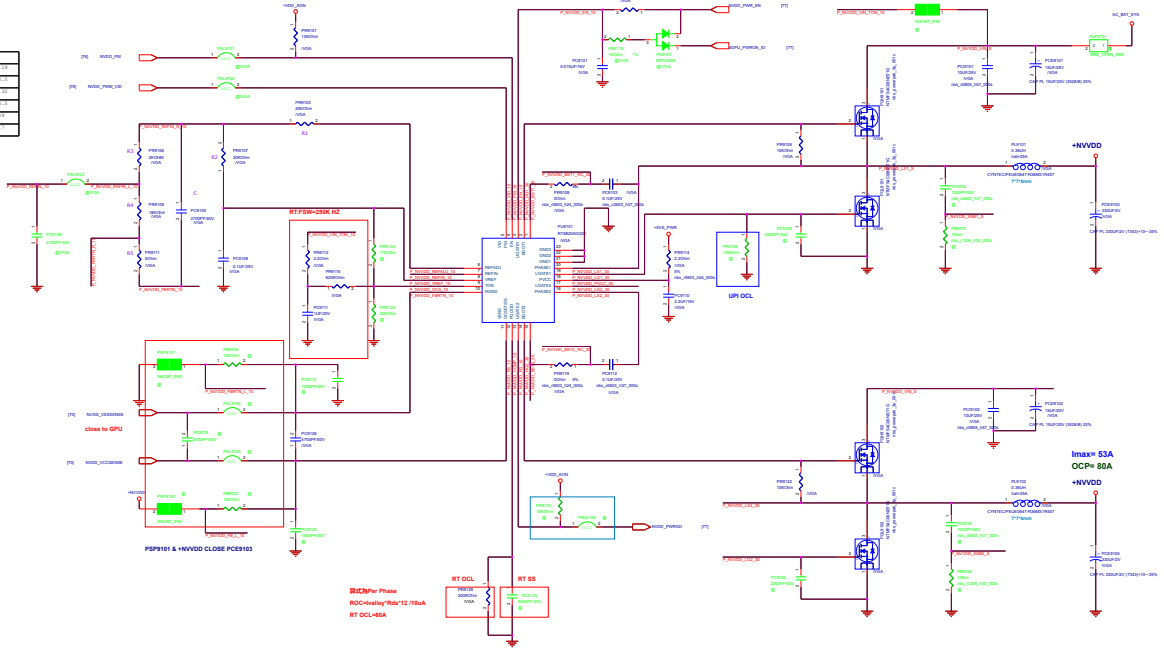
[illegible]

*+NVVDD [For DGPU]*

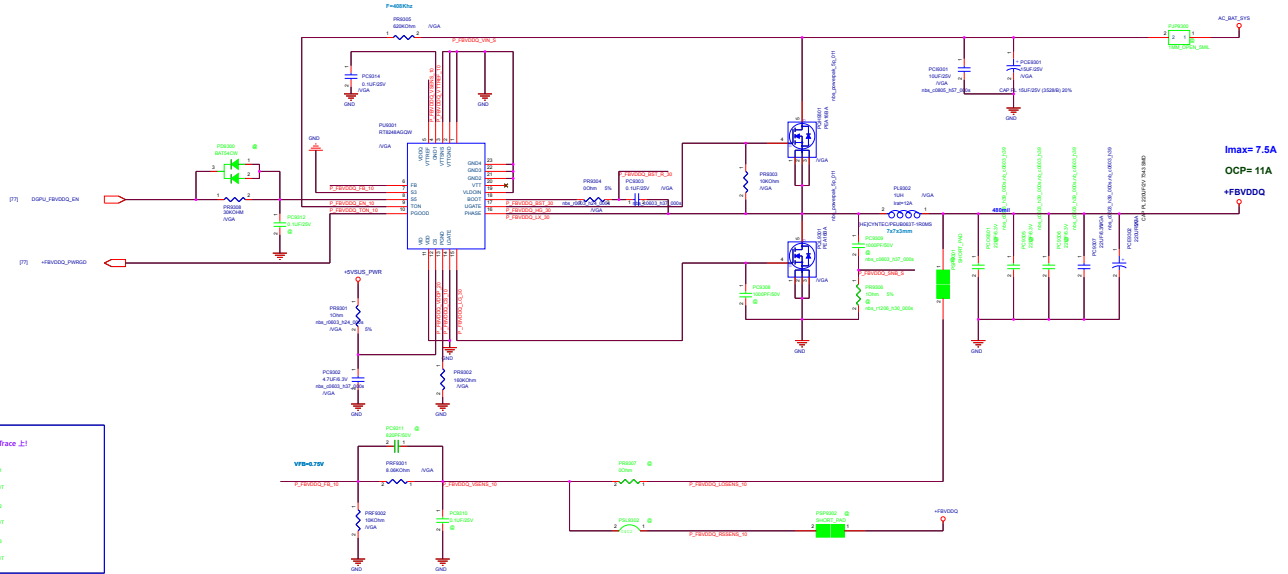


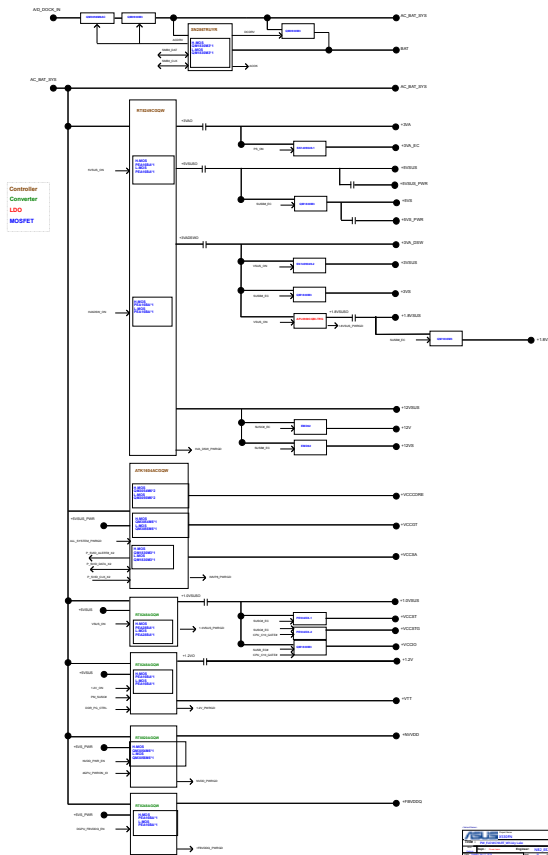
N17S Boot Voltage = 0.5V  
N16S Boot Voltage = 0.5V

	m16	m17
R1 (R100h)	20	6.18
R2 (R100h)	20	20.5
R3 (R100h)	2	4.32
R4 (R100h)	18	14.5
R5 (R100h)	0	30.9
C (CAF)	2.7	4.7

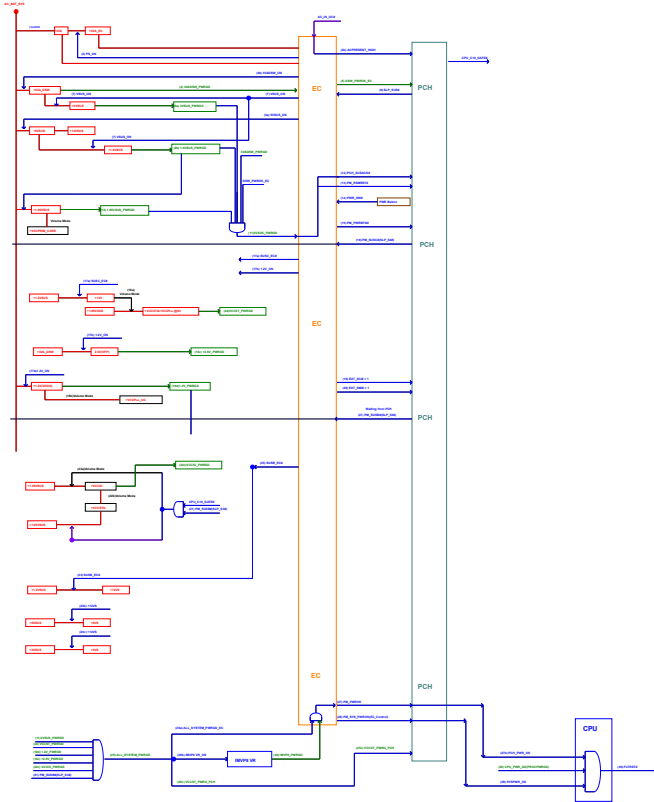


## +FBVDDQ [For VRAM]





X75FD Power On Sequence - AC mode



# X78F0 Power On Sequence - DC mode

